AMENDMENTS -- CLEAN VERSION

Presented below are the amendments in a clean, unmarked format with changes entered and not marked.

In the Specification:

Please delete the heading at page 2, line 1, and substitute the following:

#1

--KICKER FOR NON-VOLATILE MEMORY DRAIN BIAS--

In the Claims:

21. (New) --A method comprising:

providing an electrical pulse to a first drain bias circuit for a first non-volatile memory cell;

in response to the electrical pulse:

pulling a voltage of the first drain bias towards a voltage potential of a supply source; and

shorting a sense node for the non-volatile memory cell to a reference node.--

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22. (New) --The method of claim 21, wherein said first non-volatile memory cell is a flash memory cell.--

23. (New) --The method of claim 22, wherein pulling a voltage of the first drain bias towards a voltage potential of a supply voltage comprises enabling a first kicker device coupled to the drain bias for the first non-volatile memory cell.--

24. (New) --The method of claim 23, wherein said high performance transistor is a P-channel semiconductor device.--

25. (New) --The method of claim 23, wherein shorting the sense node to the reference node comprises enabling a semiconductor device coupled between the sense node and the reference node.--

26. (New) --The method of claim 25, wherein the semiconductor device comprises an s' device.--

27. (New) --The method of claim 25, wherein the electrical pulse is provided prior to sensing the contents of said first non-volatile memory cell.--

28. (New) --The method of claim 25, wherein the first non-volatile memory cell is included in a data array, and further comprising enabling a second kicker device for a second drain bias circuit for a memory cell included in a reference array, the voltage of the first drain bias circuit and a voltage of the second drain bias circuit being pulled towards the same voltage potential.--

29. (New) --The method of claim 25, wherein the first drain bias comprises a cascode amplifier.--

30. (New) --An apparatus comprising:

a kicker device, a first terminal of the kicker device being coupled to a voltage from a supply voltage and a second terminal of the kicker device being coupled to a drain bias circuit for a memory cell of a non-volatile memory device;

a semiconductor device, a first terminal of the semiconductor device being coupled to a sense node of the non-volatile memory cell and a second terminal of the semiconductor device being coupled to a reference node; and

the kicker device and the semiconductor device being enabled by an enable signal pulse.--

31. 32. (New) --The apparatus of claim 30/31, wherein the non-volatile memory device is a flash memory device.--

32. 33. (New) --The apparatus of claim 31/32, wherein the enable pulse is received prior to sensing the contents of the non-volatile memory cell.--

33. 34. (New) --The apparatus of claim 32/33, wherein the kicker device is a high performance transistor.--

34. 35. (New) --The apparatus of claim 33/34, wherein the high performance transistor is a P-channel semiconductor device.--

35. 36. (New) --The apparatus of claim 32/33, wherein the kicker pulls the voltage of a node towards the voltage potential of a supply source.--

36. 37. (New) --The apparatus of claim 32/33, wherein enabling the semiconductor device comprises equalizing the voltage potential of the sense node with the voltage potential of the reference node during bit charging.--

37. 38. (New) --The apparatus of claim 32/33, wherein the non-volatile memory drain bias circuit comprises a cascode amplifier.--

38. 36. (New) --A non-volatile memory device, comprising:

an array of memory cells;

an array of reference cells;

a first drain bias circuit for a first memory cell in the array of memory cells;

a kicker device, a first terminal of the kicker device being coupled to a voltage from a supply voltage and a second terminal of the kicker device being coupled to the first drain bias circuit;

a semiconductor device, a first terminal of the semiconductor device being coupled to a sense node of the first memory cell and a second terminal of the semiconductor device being coupled to a reference node of a first reference cell in the array of reference cells; and

the kicker device and the semiconductor device being enabled by an enable signal pulse.--

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39. 40. (New) --The non-volatile memory device of claim 38 36, wherein the non-volatile memory device is a flash memory device.--

40. 41. (New) --The non-volatile memory device of claim 39. 40, wherein the enable pulse is received prior to sensing the contents of the first memory cell.--

41. 42. (New) --The non-volatile memory device of claim 40 41, wherein the kicker device is a high performance transistor.--

42 43. (New) --The non-volatile memory device of claim 41 42, wherein the high performance transistor is a P-channel semiconductor device.--

43. 44. (New) --The non-volatile memory device of claim 42 43, wherein the kicker pulls the voltage of a node towards the voltage potential of a supply source.--

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44. 45. (New) --The non-volatile memory device of claim 40 41, wherein enabling the semiconductor device comprises equalizing the voltage potential of the sense node with the voltage potential of the reference node during bit charging.--

45. 46. (New) --The non-volatile memory device of claim 32 33, wherein the first drain bias circuit comprises a cascode amplifier.--